

CamSim-CL

Camera Link Camera Simulators



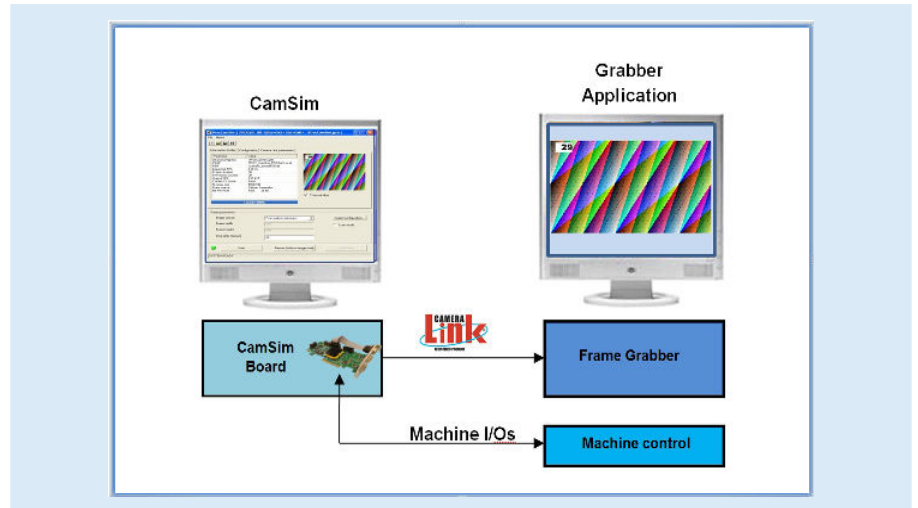
Key Features

- Simulates Camera Link image stream, including Mono, Bayer, RGB and RGBA
- Simulates all camera link v2.0 configurations (base /medium /full/80-bit (DECA))
- Supports BMP, RAW input image files
- Pattern generator for transmitting color and grayscale test patterns
- Camera Link throughput capabilities of 1-10 pixels simultaneously at 7,000-85,000 KHz. Pixel bit depth varies from 8 to 36 bits per pixel
- Fully programmable image timing and data parameter configuration via user-friendly GUI
- API methods for developing user simulator applications
- User-configurable Camera Control (CC) lines for triggering options
- Supplies machine simulator capability by adding user IOs
- Software and FPGA customization for extended machine simulation and/or custom logic/processes
- Up to 16 GB image buffer
- Two SDR-26 connectors for transmitting all camera link modes

Target Applications

- Vision Algorithms Development
- Image Processing Application Testing
- Vision System Reliability Testing
- Debugging Rare Bugs

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The Gidel **CamSim-CL™** is a flexible high-performance camera simulator that generates Camera Link video stream and test patterns for testing frame grabbers or vision/imaging systems. The system supports all Camera Link™ v2.0 configurations.

The CamSim-CL enables most development to be done in a low-cost lab environment significantly improving productivity and reducing the overall expense of developing vision and imaging systems. Gidel's CamSim-CL data flow repetition capability ensures that algorithms are validated and work as expected with pertinent input. Moreover, once the rare bug is detected, its respective data flow can be accurately reconstructed to locate the bug and quickly fix it.

The CamSim-CL suite includes:

Application Software: An intuitive GUI enabling full control of the image simulation, including: transmitting image from user files or pattern generator files and configuring the camera link and timing parameters.

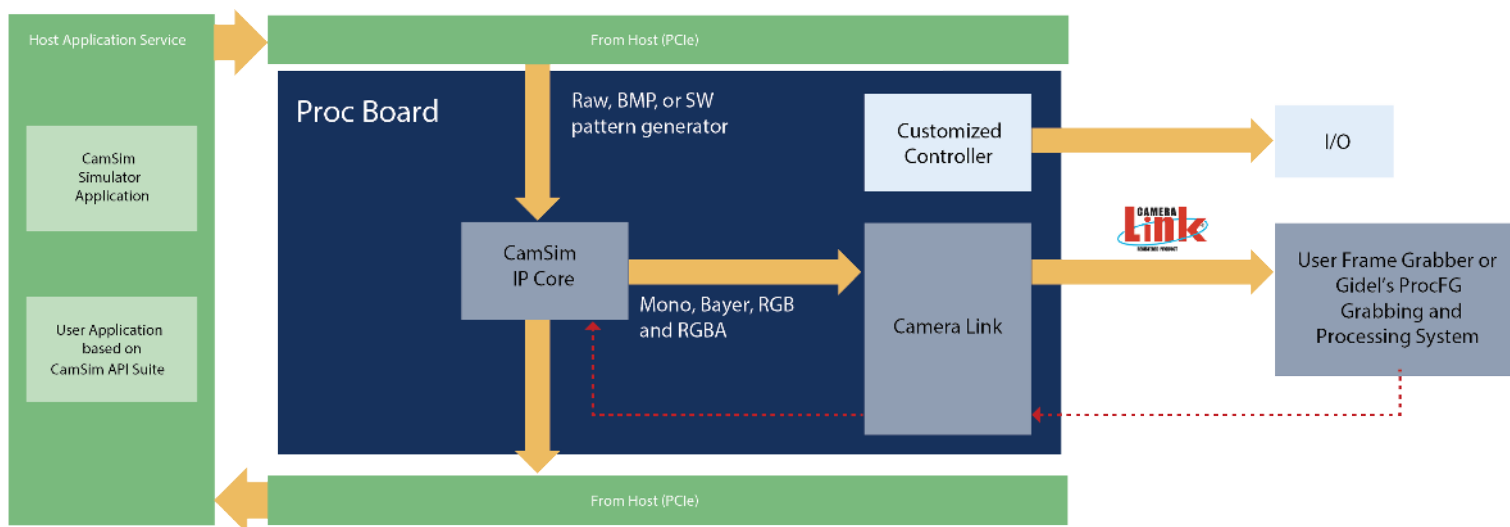
API Methods: A set of CamSim-CL API methods that can be used to develop a customized user application.

Gidel Board: A PCIe FPGA board incorporating Gidel CamSim-CL firmware for transmitting the image data.



FEATURE	SPECIFICATIONS
Camera Link Modes	1 80-bit (Deca), Full, Medium or Base Camera Link with option for PoCL
Pixel Formats	Mono, Bayer, RGBA (8, 10, 12, 14 and 16 bits/color), RGB (8, 10 and 12 bits/color)
Max. Resolution	Horizontal: 16 K pixels (24-bit) Vertical: 65 K lines (16-bit) or infinite in Line scan simulation
Camera Link Tap Configurations	All configurations as defined by the Camera Link standard, including 80-bit (Deca): 10 taps/8bits, 8bits/10taps.
Camera Link Pixel Clock	Up to 85 MHz
Connectors	2x SDR26 (mini Camera Link) VGA15-pin I/O
On-Board Memory	1-16 GB

FEATURE	SPECIFICATIONS
Host Bus	PCIe x8 Gen. 3
Host Throughput	Up to 64 Gb/s
Form Factor	PCIe low-profile
Camera Types	Area and Line
GPIO	RS422, opto-coupler, LVTTTL and 30V at 0.9A
Software Support	CamSim-CL GUI, API and examples. For open FPGA grabber version enabling customization, ProcWizard Development tool
OS Support	Win 10 /11, Server 2016/2019/2022 (64-bit) , and Linux (kernel 2.6.x- 6.12. Linux version doesn't support GUI, only API.
Certifications	RoHS, Conflict Minerals, ISO
Operating Ambient Temperature	0 – 55 C, relative humidity up to 90%
MTBF	> million hours



CamSim-CL System Overview